AMENDED CLAIMS

What is claimed is:

1. (currently amended) A method of detecting overflow in a clamping circuit, comprising:

inputting a first operand having a first fixed-point format into the clamping circuit;

inputting a second operand having a second fixed-point format into the clamping circuit;

determining an overflow output based upon the first and second fixed-point format and predicting whether an arithmetic operation of the first operand with the second operand will yield a result that exceeds the overflow output; ~~and~~

performing at least partially the arithmetic operation of the first and second operands;

inputting the result and overflow output into a multiplexor for selection therebetween; and

discontinuing the performing if the result exceeds the overflow output;

wherein the determining and predicting occurs independent from and substantially in parallel with the performing.

2. (currently amended) A method of detecting overflow in a clamping circuit, comprising:

inputting a first operand having a first fixed-point format into the clamping circuit;

inputting a second operand having a second fixed-point format into the clamping circuit;

determining a product overflow output based upon the first and second fixed-point format and predicting whether multiplication of the first operand with the second operand yields a result that exceeds the product overflow output; ~~and~~

performing at least partially the multiplication of the first and second operands;

inputting the result and product overflow output into a multiplexor for selection therebetween; and

discontinuing the performing if the result exceeds the product overflow output;

wherein the determining and predicting occurs independent from and substantially in parallel with the performing.

3. (currently amended) A method of clamping fixed-point multipliers, comprising:

providing a first operand in a first fixed-point format;

providing a second operand in a second fixed-point format;

at least partially multiplying the first operand with the second operand to produce an operation result;

determining whether the operation result will exceed a representable value;

determining a clamping value based on the first fixed-point format of the first operand and the second fixed-point format of the second operand; ~~and~~

substituting the operation result with the clamping value when it is determined that the operation result will exceed the representable value;

inputting the operation result into a multiplexor; and

discontinuing the multiplying if the operation result exceeds the representable value;

wherein the multiplying and determining whether the operation result will exceed the representable value occur independently and substantially in parallel.

4. (previously presented) A method of clamping fixed-point multipliers, comprising:

providing a first and second input operand;

determining a desired number of output bits;

where any of the first and second input operands are positive, counting a number of leading logical zeros in the positive operands;

where any of the first and second input operands are negative, counting a number of leading logical ones in the negative operands;

summing the number of leading logical zeros of the positive operands with the number of leading logical ones in the negative operands;

determining a clamping decision based on the summing to yield a simple clamp predictor representative of the clamping decision;

computing a product of the first operand and the second operand such that the product has the desired number of output bits plus one additional bit; and

logically ORing the simple clamp predictor with a most significant bit of the product.